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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/595,860	06/16/00	BERTHOLD	~~GR-97-P-6457~~

EXAMINER	
NGUYEN, C	

ART UNIT	PAPER NUMBER
2871	

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08/29/01

Please find below and/or attached an Office communication concerning this application or pr ceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application N.	Applicant(s)	
09/595,860	BERTHOLD et al.	
Examiner	Group Art Unit	
CUONG Q NGUYEN	2811	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Dispositi n of Claims

☒ Claim(s) 1-24 is/are pending in the application.

Of the above claim(s) 24 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-23 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Applicati n Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ Th drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group I, claims 1-23 in Paper No.8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

2. The oath/declaration filed on 06/16/00 is acceptable.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 06/16/00 has been considered.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claims 1-7, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Bothra et al. (US 5,798,559).

Regarding claims 1, 3- 7, Bothra et al. discloses an integrated circuit comprising: a plurality of structure planes on which the metalizations (38, 154, 118) are formed; the structure planes including an element structure plane (a substrate 100); electrically active elements (the MOS transistor not shown in the figures. See Bothra et al.'s col.1, lines 15-20) formed on the element structure plane; an insulation layer (120, a semiconductor oxide layer. Bothra et al.'s col.6 lines 9-20) formed above the element structure plane; electrical connecting leads (metalizations 118 of pure Cu. See Bothra et al.'s col.5, lines 39-53) formed within the insulation layer; connection pieces (114, 110) formed underneath the electrical connecting leads (118); a diffusion blocker (116) of silicon nitride (Bothra et al.'s col.4, lines 51-58) formed between insulation layer (1200 and the element structure plane, wherein the diffusion blocker is interrupted only a region having contact holes. See Bothra et al.'s Fig.3K.

It is noted that the diffusion blocker (116) formed of silicon nitride the same material the diffusion blocker in the present invention. Therefore, it is inherent that the diffusion blocker in Bothra et al. has capability of preventing a diffusion of copper as claimed.

Regarding claims 2 and 18, as shown in Bothra et al.'s Fig.3K and col.5 lines 60-65), diffusion barriers of TiN for impeding a diffusion of copper formed on a surface of connection pieces and on surfaces of electrical connecting leads (118).

Chiang et al. does not teach that electrically active elements formed on the element structure plane (the substrate) and more than one connection pieces (the plugs) formed underneath the electrical connecting leads.

It is conventional and also taught by Oda, Hayashide, Tottori that a plurality of electrically active elements such as MOS transistors formed on the substrate and a plurality of plugs formed underneath the metalizations (the electrical connecting leads) in the integrated circuit

It would have been obvious to one of ordinary skill in the art to form a plurality of MOS transistor on the substrate and a plurality of conductive plugs in contact holes as taught by Oda, Hayashide and Tottori in Chiang et al.'s device because in the integrated circuit a thousands or millions of MOS transistor and conductive plugs connecting to sour/drain of the MOS transistor are commonly formed on the substrate to form the memory semiconductor device.

It is noted that the diffusion blocker (23) formed of silicon nitride the same material the diffusion blocker in the present invention. Therefore, it is inherent that the diffusion blocker in Chiang et al. has capability of preventing a diffusion of copper as claimed.

Regarding claim 2, as shown in Chiang et al.'s Fig.12, diffusion barriers (40) of TiN for impeding a diffusion of copper formed on a surface of contact hole.

Regarding claim 7, Chiang et al. teaches that the blocker layer is formed of silicon nitride. However, Chiang et al. does not explicitly teach that the silicon nitride is Si3N4.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of Si3N4 as claimed because Si3N4 is commonly used to form silicon nitride layer in the semiconductor device.

Regarding claim 15, as shown in Chiang et al.'s Fig. 12, the blocker layer (23) is one of a plurality of blockers.

Regarding claim 16, as shown in Chiang et al.'s Fig. 12, a second blocker layer (123) formed on a different structure plane than the blocker layer (23).

Regarding claims 17 -20, as shown in Chiang et al.'s Fig. 12, the blocker layers (121) and (40) impede the diffusion and prevent diffusion, wherein the further diffusion blocker (121) is on the side areas and on the lower edges of electrical connecting leads (120) to prevent bulk outdiffusion of copper into the insulation layer (122). Because one blocker has different thickness than another one, therefore the diffusion prevention of the block layers are different.

Regarding claim 21, as shown in Chiang et al.'s Fig. 12, the blocker layer (23) is greater than the further blocker layer (40).

Regarding claim 22, the blocker layer (23) has a thickness of 1000 angstroms (Chiang et al.'s col.8 lines 9-11) greater than a thickness of the further blocker (40) of 500 angstroms (Chiang et al.'s col.8 line 30).

Regarding claim 23, Chiang et al. does not teach that a diffusion through the blocker layer (23) is less than 10% of a diffusion through the further diffusion blocker (40). However, the diffusion through the blocker layer is depending on the thickness of the blocker.

Therefore, it would have been obvious to one of ordinary skill in the art to form the blocker layers such as the blocker layer (23) is less than 10% of a diffusion through the further diffusion blocker (40) as claimed because the thickness of layers (23) and (40) are art recognized variable of importance which is subject to routine experimentation and optimization.

Claims 8, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. in view of Oda, Hayashide, Tottori and further in view of Hong (US 6,008,117).

Chiang et al., Oda, Hayashide, Tottori teach all the limitations of claims 1-7, and 14-23 as shown above. However, above prior arts do not teach that the blocker layer is formed of silicon oxynitride or metal oxide such as TiO2.

Hong discloses an integrated circuit comprising a blocker layer (14) is formed of silicon nitride or silicon oxynitride or TiO2. See Hong's Fig.1H and col.2 lines 52-56.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of silicon oxynitride or TiO2 instead of silicon nitride as taught by Hong because materials such as silicon nitride, silicon oxynitride and TiO2 are commonly used to form the blocker layer in the semiconductor device and they are interchangeable.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. in view of Oda, Hayashide, Tottori , Hong and further in view of McCollum et al. (US 5,552,627).

Chiang et al., Oda, Hayashide, Tottori teach all the limitations of claims 1-9, and 12-23 as shown above. However, above prior arts do not teach that the blocker layer is formed of a fluorinated nitride such as fluorooxynitride.

McCollum et al. discloses an integrated circuit comprising a blocker layer formed of fluorinated nitride material by deposited the silicon nitride using an NF3 atmosphere in the reactor. McCollum et al. teaches that fluorinated nitride has a lower leakage than a similar nitride material. See McCollum et al.'s Fig.3 and col.8, lines 42-51.

Therefore, it would have been obvious to one of ordinary skill in the art to form the block layer of silicon nitride or silicon oxynitride by deposited the silicon nitride using an NF3 atmosphere as taught by McCollum et al. in order to reduce the leakage of the blocker layer.

It is inherent that the silicon oxynitride is formed by deposited the silicon nitride using an NF3 atmosphere would produce fluorinated nitride such as fluorooxynitride.

Conclusion

7. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

8. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Tom Thomas

CN

August 24, 2001

TOM THOMAS
SUPERVISORY PATENT EXAMINER